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(12) # EUROPEAN PATENT APPLICATION

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(54) **High speed, low gate/drain capacitance dmos device.**

(57) A DMOS device (30) with field oxide (46) formed in the channel between adjacent transistors and an impurity (44) implanted through the same opening in which the field oxide is formed. The gate (50) is deposited over the field oxide (46) and spaced from the supporting epitaxial layer (34) by the field oxide (46) to reduce the gate-to-drain capacitance. The implanted impurity (44) below the field oxide (46) reduces ON resistance of the device (30).

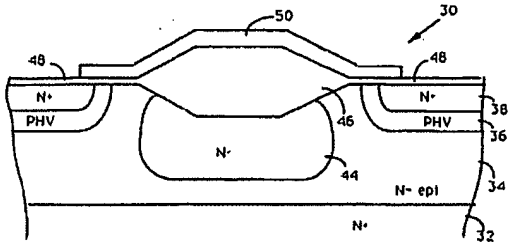

FIG 6

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The present invention pertains to double diffused metal oxide semiconductor devices and more specifically to high speed vertical double diffused metal oxide semiconductor devices in which the gate to drain capacitance and the ON resistance are substantially reduced.

Background of the Invention

In general, vertical double diffused metal oxide semiconductor (DMOS) devices have a gate spaced from the active junction by a layer of gate oxide approximately 500 - 1000 angstroms thick. Because the gate is very close to the active junction and the channel, or drain, of the device, a relatively large capacitance, C_{GD}, is formed between the gate and the drain of the device. This capacitance acts as a negative feedback path and limits the speed of switching of the device

Further, in higher voltage vertical DMOS devices an epitaxial layer on the substrate in which the devices are formed is relatively lightly doped. This lightly doped region in the conductive path of the device increases the resistance of the device in the ON mode.

Summary of the Invention

It is a purpose of the present invention to provide a new and improved method of producing high speed, low gate/drain capacitance DMOS devices.

It is a further purpose of the present invention to provide a new and improved method of producing high speed, low gate/drain capacitance DMOS devices with low ON resistance.

These and other purposes and advantages are realized in a method of producing high speed, low gate/drain capacitance DMOS devices, including the steps of providing a substrate forming a first layer of material having a first conductivity type on a surface of the substrate, diffusing first and second spaced apart areas of a second conductivity type, different than the first conductivity type, into the first layer, diffusing first and second spaced apart areas of the first conductivity type into the first and second areas of the second conductivity type, forming a relatively thick layer of insulating material on the first layer of material between the first and second spaced apart areas of the second conductivity type, forming a relatively thin layer of insulating material over the relatively thick layer of insulating material, the first and second spaced apart areas of the second conductivity type and the first and second spaced apart areas of the first conductivity type, and forming a gate layer over the relatively thin layer of insulating material in overlying relationship to the relatively thick layer of insulating material, a portion of the first and second spaced apart areas of the second conductivity type and a portion of the first and second spaced apart areas of the first conductivity type.

Brief Description of the Drawings

Referring to the drawings:

FIG.1 is a cross sectional view of a prior art DMOS device;

FIG.2 is a schematic depiction of a DMOS device; and

FIGS. 3 - 6 are cross sectional views illustrating various steps in the manufacture of a DMOS device in accordance with the present invention.

Description of the Preferred Embodiment

Referring specifically to FIG. 1, a cross sectional view of a prior art DMOS device 10 is illustrated. Device 10 is formed on a silicon substrate 12 which is relatively heavily doped to produce N type conductivity. An epitaxial layer 14 is grown on the surface of substrate 12 and is lightly doped to produce N type conductivity. P type conductivity tubs 16 are diffused into epitaxial layer 14 and heavily doped N type conductivity 18 is diffused into tubs 16 to form N-P-N junctions in epitaxial layer 14. The area 22 between tubs 16 from the surface of epitaxial layer 14 to a depth less than the depth of tubs 16 is heavily doped to reduce the resistance of the final device in the ON mode. Finally, a very thin layer 20 of gate oxide is grown over the entire surface of epitaxial layer 14 and a gate 25 is deposited on layer 20 in overlying relationship to portions of tubs 16, portions of conductivity 18 and area 22.

Referring specifically to FIG. 2, a schematic representation of a DMOS device, which in this instance is a field effect transistor (FET). The DMOS device includes a source electrode labelled S, a drain electrode labelled D and a gate electrode labelled G. As is well known in the art and as can be seen from the schematic depiction of FIG. 2, a capacitance C_{GD} is present between drain electrode D and gate electrode G. Capacitance C_{GD} provides feedback from drain electrode D to gate electrode G which limits the switching speed of the DMOS device. In DMOS device 10 of FIG. 1, layer 20 is on the order of 500 - 1000 angstroms thick so that gate 25 is very close to the drain, or channel 22. Capacitance C_{GD} is primarily produced by conductive gate 25 and heavily doped conductive area 22 with insulating layer 20 therebetween. In DMOS device 10 capacitance C_{GD} is relatively large and the speed of DMOS device 10 is severely limited.

FIGS. 3 - 6 are cross sectional views illustrating various steps in the manufacture of a DMOS

device 30 in accordance with the present invention. Referring specifically to FIG. 3, a substrate 32 is heavily doped with N type conductivity impurities and an epitaxial layer 34 is grown on the surface thereof. Epitaxial layer 34 is relatively lightly doped to provide for higher breakdown voltages.

A thin protective layer 39 of oxide is grown on the surface of epitaxial layer 34 and is generally retained throughout the procedures described thus far. A layer 41 of silicon nitride is deposited over layer 39 and patterned by any convenient means, such as well known photoresist and etch processes, to define an opening 42 therethrough. In this particular embodiment layer 41 is formed approximately 1400 angstroms thick so that it masks everything but opening 42 during subsequent process steps.

Referring specifically to FIG 4, the structure of FIG. 3 is illustrated with an impurity or dopant being implanted, represented by arrows 44, into epitaxial layer 34 through opening 42. Implant 44 may be diffused by a specific diffusion step or by subsequent process steps.

Referring specifically to FIG. 5, the structure of FIG. 4 is illustrated with the next step in the process performed. A relatively thick layer 46 of insulating material, which in this specific embodiment is a field oxide, is grown in opening 42 on the surface of epitaxial layer 34. Layer 46 is at least 1000 angstroms thick and can be as much as 10,000 angstroms thick. In this specific embodiment layer 46 is approximately 5000 angstroms thick. Diffused implant 44 is positioned directly below layer 46 . Thus, implant 44 is self aligned and implant 44 and relatively thick layer 46 are both formed by using opening 42 and no additional masking steps are required.

Referring specifically to FIG. 6, the structure of FIG. 5 is illustrated with layers 41 and 39 removed and a layer 48 of gate oxide grown over the entire surface of epitaxial layer 34, including layer 46. While gate oxide growth will have relatively little effect on layer 46, it is included only so it will be understood that no masking or other steps are utilized. Once layer 48 is grown, a gate 50 is deposited on the surface of layer 48 in partially overlying relationship to layer 46.

After gate layer 50 is formed, first and second spaced apart areas 36 of a P type conductivity are implanted and diffused into epitaxial layer 34 using layer 46 and gate layer 50 as a mask. Areas 36 are relatively lightly doped to form the channel of DMOS device 30, hence the designation PHV. First and second relatively heavily doped areas 38 of N type conductivity are implanted and diffused in first and second areas 36, respectively. Each of areas 38, in conjunction with the associated area 36 and epitaxial layer 34 form an N-P-N junction.

It should be understood that the structure illustrated in FIG. 6 is only a small part of the complete device and, if viewed from the top, would appear as a plurality of cells (extending into FIG. 6). FIG 6 illustrates approximately one half of a left cell and one half of a right cell.with the broken away halves being mirror images of the portions illustrated. Further, first and second areas 36 with first and second areas 38 implanted therein and the or portion of epitaxial layer 34 defined therebetween, each form one half of two separate transistors, the broken away portions of the cells being the other half.

Because gate 50 is spaced from epitaxial layer 34 by the thickness of layer 46, except for a small portion immediately adjacent the N-P-N junction formed by areas 38, areas 36 and epitaxial layer 34, the capacitance CGD is greatly reduced and the speed of DMOS device 30 is greatly improved. Further, implant 44 provides a relatively low resistance to current for a substantial portion of the current path through DMOS device 30. Also, by spacing implant 44 from areas 36, or at least the heavily doped portions thereof, the breakdown voltage of DMOS device 30 is not effected. Because implant 44 and relatively thick layer 46 are formed with the same nitride layer 41, the entire process is relatively simple and self aligned to insure accurate placement of the described components. Thus, a new and improved method of producing high speed, low gate/drain capacitance DMOS devices is disclosed. Also, a new and improved method of producing high speed, low gate/drain capacitance DMOS devices with low ON resistance is disclosed which is incorporated without requiring additional masking or alignment steps.

Claims

1. A high speed, low gate/drain capacitance DMOS device including a substrate (32), a first layer (34) of material formed on a surface of the substrate (32) having a first conductivity type, first and second spaced apart areas (36) of a second conductivity type, different than the first conductivity type, diffused into the first layer (34), and first and second spaced apart areas (38) of the first conductivity type diffused into the first and second areas (36) of the second conductivity type, the device being characterized by:

   a dopant (44) implanted into an area between, and spaced from, the first and second spaced apart areas (36) of a second conductivity type to produce a relatively highly conductive area of the first conductivity type;

   a relatively thick layer (46) of insulating material formed on the first layer (34) of ma-

terial between the first and second spaced apart areas (36) of a second conductivity type and overlying the implanted dopant (44);

a relatively thin layer (48) of insulating material formed on the relatively thick layer (46) of insulating material, the first and second spaced apart areas (36) of the second conductivity type and the first and second spaced apart areas (38) of the first conductivity type; and

a gate layer (50) formed over the relatively thin layer (48) of insulating material in overlying relationship to the relatively thick layer (46) of insulating material, a portion of the first and second spaced apart areas (36) of the second conductivity type and a portion of the first and second spaced apart areas (38) of the first conductivity type.

2. A high speed, low gate/drain capacitance DMOS device as claimed in claim 1 further characterized in that the relatively thick layer (46) of insulating material includes an oxide.

3. A high speed, low gate/drain capacitance DMOS device as claimed in claim 1 further characterized in that the relatively thick layer (46) of insulating material is greater than approximately 1000 angstroms thick.

4. A high speed, low gate/drain capacitance DMOS device as claimed in claim 1 further characterized in that the relatively thick layer (46) of insulating material is in the range of approximately 5000 to 6000 angstroms thick.

5. A high speed, low gate/drain capacitance DMOS device as claimed in claim 1 further characterized by a patterned layer (41) of material formed on the first layer (34) of material and defining an opening (42) between the first and second spaced apart areas (36) of a second conductivity type and wherein the relatively thick layer (46) of insulating material includes an oxide grown in the opening (42).

6. A method of producing high speed, low gate/drain capacitance DMOS devices, including the steps of providing a substrate (32) and forming a first layer (34) of material having a first conductivity type on a surface of the substrate (32), the method characterized by:

forming a relatively thick layer (46) of insulating material on the first layer (34) of material;

forming a relatively thin layer (48) of insulating material over the relatively thick layer of insulating material;

forming a gate layer (50) over the relatively thin layer (48) of insulating material in overlying relationship to the relatively thick layer (46) of insulating material;

diffusing first and second spaced apart areas (36) of a second conductivity type, different than the first conductivity type, into the first layer (34), the first and second spaced apart areas (36) being separated by the relatively thick layer (46) of insulating material and positioned on opposite sides thereof; and

diffusing first and second spaced apart areas (38) of the first conductivity type into the first and second areas (36) of the second conductivity type, the first and second spaced apart areas (36) of the second conductivity type and the first and second spaced apart areas (38) of the first conductivity type being positioned so that the relatively thin layer (48) of insulating material and a portion of the gate layer (50) overlie a portion of the first and second spaced apart areas (36) of the second conductivity type and a portion of the first and second spaced apart areas (38) of the first conductivity type

7. A method of producing high speed, low gate/drain capacitance DMOS devices as claimed in claim 6 further characterized in that the step of forming a relatively thick layer (46) of insulating material includes the steps of depositing a layer (41) of nitride over the first layer (34) of material, patterning the layer (41) of nitride to define an opening (42) therethrough between the first and second spaced apart areas (36) of the second conductivity type, and growing a relatively thick layer (46) of field oxide on the first layer (34) of material in the opening (42).

8. A method of producing high speed, low gate/drain capacitance DMOS devices as claimed in claim 7 further characterized by the step of implanting an impurity (44) through the opening (42) into the first layer (34) of material prior to the step of growing the relatively thick layer (46) of field oxide.

9. A method of producing high speed, low gate/drain capacitance DMOS devices as claimed in claim 7 further characterized in that the step of growing a relatively thick layer (46) of field oxide includes growing a layer of field oxide with a thickness greater than approximately 1000 angstroms.

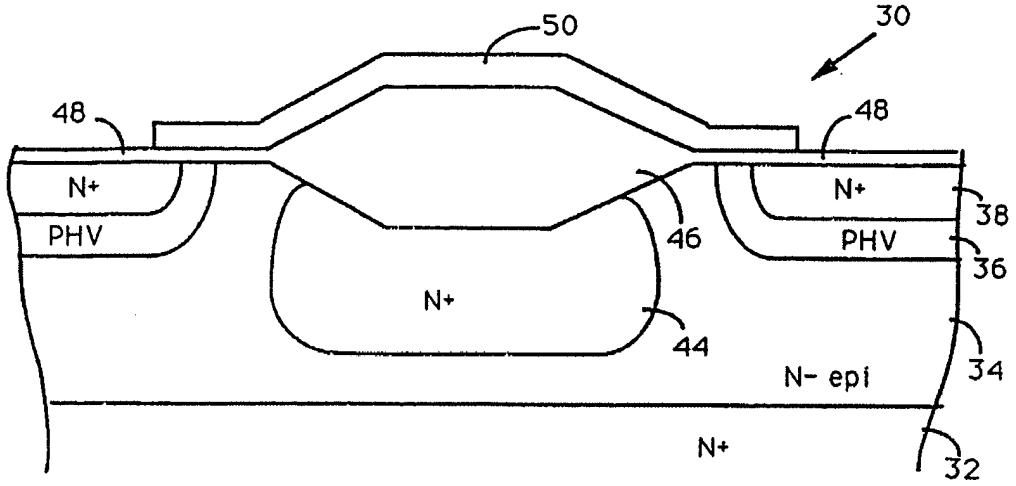

FIG. 6

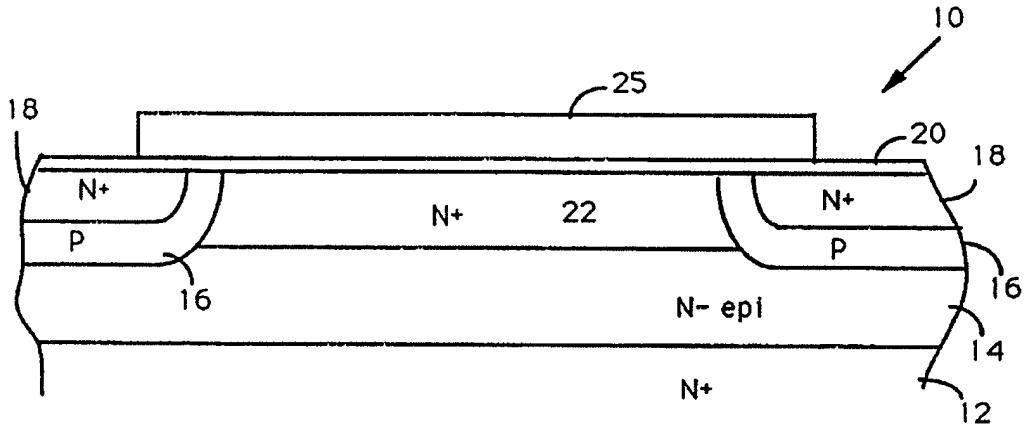

FIG. 1

PRIOR ART

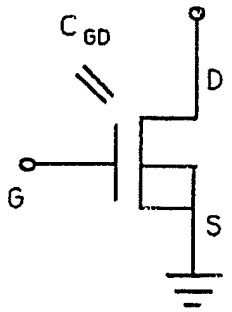

FIG. 2

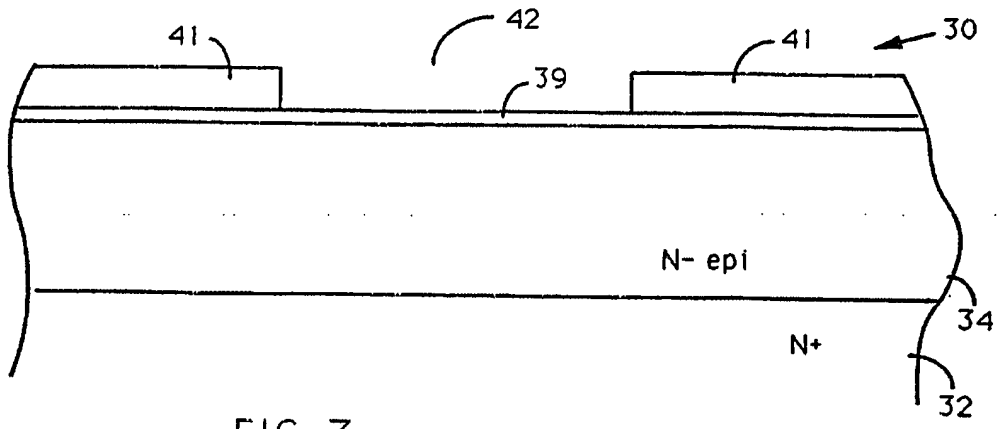

FIG. 3

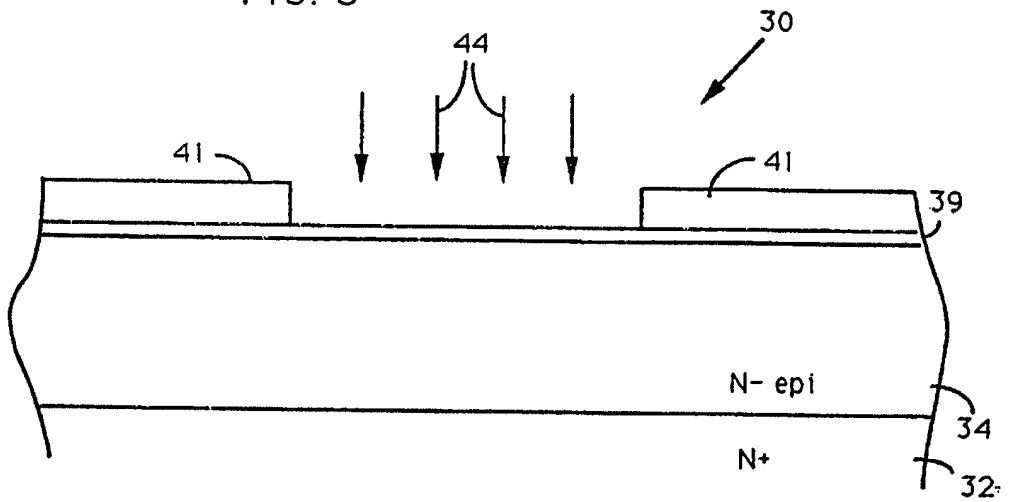

FIG. 4

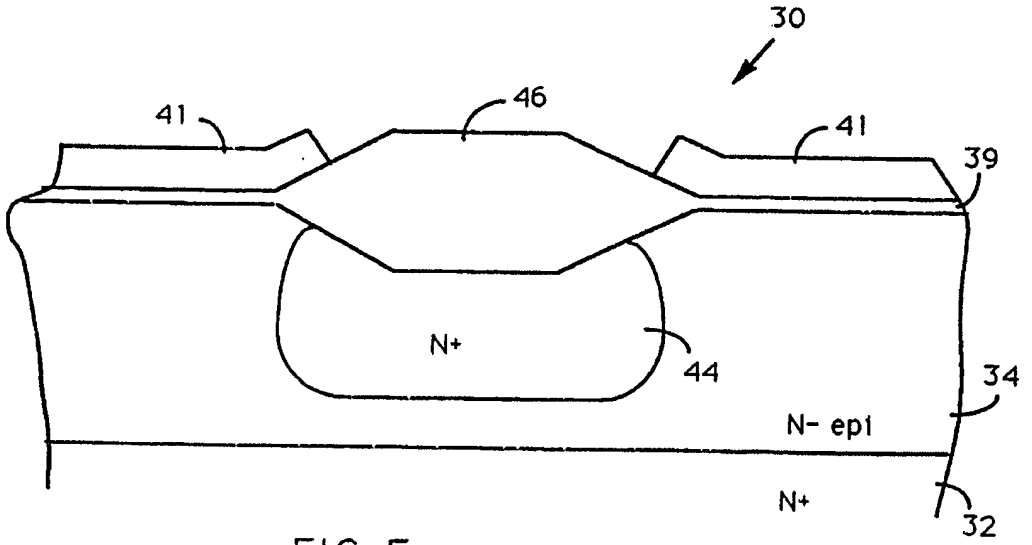

FIG. 5

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EUROPEAN SEARCH REPORT

Application Number
EP 93 11 1360

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X Y	EP-A-0 050 773 (SIEMENS) * page 2, line 24 - page 4, line 34; figures 1,2 *	1-3 4,5,8,9	H01L29/60
X Y	PATENT ABSTRACTS OF JAPAN vol. 14, no. 371 (E-963)(4314) 10 August 1990 & JP-A-21 33 966 (FUJI ELECTRIC) 23 May 1990 * the whole document *	6,7 5,8,9	
X Y	WO-A-9 111 826 (F.L. QUIGG) * page 8, line 12 - page 12, line 30; figures 5-12 *	6 4	
A	EP-A-0 420 485 (LUCAS INDUSTRIES PUBLIC) * figure 4 *	1	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	28 SEPTEMBER 1993	JUHL A.

CATEGORY OF CITED DOCUMENTS

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